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600 13th Street, N.W.
Washington, DC 20005-3096

EXAMINER

NGUYEN, THANH T

ART UNIT PAPER NUMBER

2813

DATE MAILED: 11/01/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/817,056

Applicant(s)

YANG ET AL.

Examiner

Thanh T. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 September 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) 13-23 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 6-12 is/are allowed.
- 6) ☒ Claim(s) 1-5, 24-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

Request for Continued Examination

The request filed on 9/14/04 for a Request for Continued Examination (RCE) under 37 CFR 1.114 is acceptable and a RCE has been established. An action on the RCE follows.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(e) the invention was described in-

(1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effect under this subsection of a national application published under section 122(b) only if the international application designating the United States was published under Article 21(2)(a) of such treaty in the English language; or

(2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that a patent shall not be deemed filed in the United States for the purposes of this subsection based on the filing of an international application filed under the treaty defined in section 351(a).

Claims 1-2 and 4-5 are rejected under 35 U.S.C. 102(e) as being anticipated by Chooi et al. (U.S. Patent No. 6,284,657).

Referring to figures 1, 4-8, Chooi et al. teaches a method of manufacturing a semiconductor device:

Forming a single first dielectric layer (14) overlying a substrate (10, see figure 1 and col. 5, lines 24-48),

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Forming a first barrier layer (16, a silicon nitride layer, SiN, meeting claim 2), comprising a first dielectric barrier material of silicon nitride (20) on the single first dielectric layer (14),

Etching to form a single opening (25) entirely within and defined by side surfaces and a bottom of the single first dielectric layer and a bottom (14, see figure 4),

Forming a second barrier layer (15, a silicon carbide layer, SiC, called a “non-metallic layer” in Chooi et al., see figures 5, col. 6, lines 21-33, meeting claim 2), comprising a second dielectric barrier material of SiC (15) different from the first dielectric barrier material of silicon nitride (16, SiN), on an entire upper surface of the first barrier layer (16, figure 5, wherein the second dielectric barrier (15) is on entire upper surface of the barrier layer (16)) overlying the single first dielectric layer (14), on the side surfaces of the first dielectric layer (14) defining the first opening and on the bottom of the opening (25),

Etching, with selectivity to the first barrier layer (16), to remove the second barrier layer (15) from, and stopping on, the upper surface of the first barrier layer (16), and to remove the second barrier layer (15) from the bottom of the single opening (25), leaving a portion of the second barrier layer (15) as a liner (19) on the side surfaces of the single first dielectric layer (14) defining the single opening (25, see figure 6, col. 6, lines 34-49), and

Filling the opening with metal (copper, meeting claim 5) to form a lower metal feature (see col. 7, lines 5-7),

In regarding to claim 3, depositing second barrier layer of silicon carbide (15) by chemical vapor deposition (CVD, see col. 6, lines 23-33, meeting portion of claim 3),

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In regarding to claim 4, depositing first barrier layer of silicon nitride (16, SiN) at a thickness of between 500-5,000 Å (see col. 5, lines 35-45) and second barrier layer of silicon carbide (15) at the thickness of between 50-5,000 Å (see col. 6, lines 23-33).

Claims 24-26 are rejected under 35 U.S.C. 102(e) as being anticipated by Chooi et al. (U.S. Patent No. 6,284,657).

Referring to figures 10-14, Chooi et al. teaches a method of manufacturing a semiconductor device:

Forming a single non-fluorinated first dielectric layer (14, see col. 7, lines 62-67, col. 8, lines 1-5) overlying a substrate (10, see figure 10),

Forming a first barrier layer (16, a silicon nitride layer, SiN), comprising a first dielectric barrier material of silicon nitride (20) on the single first dielectric layer (14),

Etching to form a single opening (figure 11, col. 8, lines 12-29) entirely within and defined by side surfaces and a bottom of the single first dielectric layer and a bottom (14, see figure 11),

Forming a second barrier layer (26, a silicon carbide layer, SiC, called a “non-metallic layer” in Chooi et al., see figures 12, col. 8, lines 30-42), comprising a second dielectric barrier material of SiC (26) different from the first dielectric barrier material of silicon nitride (16, SiN), on an entire upper surface of the first barrier layer (16, figure 5, wherein the second dielectric barrier (26) is on entire upper surface of the barrier layer (16)) overlying the single first dielectric layer (14), on the side surfaces of the first dielectric layer (14) defining the first opening and on the bottom of the opening (see figure 12),

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Etching, with selectivity to the first barrier layer (16), to remove the second barrier layer (26) from, and stopping on, the upper surface of the first barrier layer (16), and to remove the second barrier layer (26) from the bottom of the single opening (see figure 13), leaving a portion of the second barrier layer (26) as a liner (19) on the side surfaces of the single first dielectric layer (14) defining the single opening (see figure 13, col. 8, lines 53-67), and

Filling the opening with metal (copper, meeting claim 26) to form a lower metal feature (see figure 14, col. 9, lines 7-18),

In regarding to claim 25, depositing first barrier layer of silicon nitride (16, SiN) at a thickness of between 500-5,000 Å (see col. 8, lines 4-7) and second barrier layer of silicon carbide (26) at the thickness of between 50-5,000 Å (see col. 8, lines 30-36).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Chooi et al. (U.S. Patent No. 6,284,657) as applied to claims 1-2 and 4-5 above, and further in view of Chung et al. (U.S. Patent No. 6,017,817).

Chooi et al. teaches using silicon nitride layer as a cap layer (first barrier layer) and silicon carbide as a second barrier layer as shown in figures 1 and 4, but fails to teach that

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depositing a silicon nitride layer by a Chemical vapor deposition method (CVD, as claimed in claim 3). Nevertheless, such processing step is known in the semiconductor processing art as evidenced by Chung et al. Chung et al. teach a method of forming a silicon nitride (208) cap layer by using CVD process (see col. 3, lines 25-29 and figure 2A).

Therefore, it would have been obvious to a person of ordinary skill in the requisite art at the time the invention was made would depositing a silicon nitride layer as first barrier layer and silicon carbide as second barrier layer by a CVD method in Chooi et al.'s process as taught by Chung et al. *because* depositing a silicon nitride layer by CVD process would provide a film layer having good thickness uniformity, high purity and good step coverage.

Allowable Subject Matter

Claims 6-12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims because inter alia the prior art of record fails to disclose nor suggest to combine forming a third dielectric barrier layer on the first barrier layer and on upper surface of the lower metal feature, a second dielectric layer on the third dielectric barrier layer, a fourth dielectric barrier layer on the second dielectric layer, forming a third dielectric layer on the fourth dielectric barrier layer, forming a fifth dielectric barrier layer on the third dielectric layer, etching to form a dual damascene opening in the second and third dielectric layers over the lower metal feature, forming a sixth dielectric barrier layer comprising a sixth dielectric barrier material different from the first, fourth and fifth dielectric layers in the dual damascene opening,

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and filling the dual damascene opening with metal to form a metal line connected to an underlying metal via in the claimed invention as a whole.

Response to Arguments

Applicant's arguments filed 9/14/04 have been fully considered but they are not persuasive.

Applicant contends that Chooi et al. does not teach form a second barrier layer on an entire upper surface of the first barrier layer. In response to applicant that Chooi et al. clearly teaches forming a second barrier layer on an entire upper surface of the first barrier layer (see figure 5, wherein the barrier (15) is formed on an entire upper surface of the first barrier layer as well as the layers 18 and 20).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (703) 872-9306.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (See **MPEP 203.08**).

A handwritten signature in black ink, appearing to read 'Thanh', with a long horizontal stroke extending to the left.

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800